STM32H7 SOM (System-On-Module)

Hardware Architecture

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1. Introduction

This document describes the hardware architecture of the Emcraft Systems STM32H7 SOM (System-On-Module).

The STM32H7 SOM is intended to provide a flexible platform for embedded applications that require rich connectivity, low power and flexibility of the STM32H750 coupled with a full-fledged uClinux software execution environment running on the ARM Cortex-M7 processor core.

The STM32H7 SOM is based on the ST Microelectronics STM32 H750 versatile, low-power, high-integration microcontroller.

Using a miniature form factor, the STM32H7 SOM is specifically designed for surface-mounting on the OEM PCB. It has castellated pads to allow for easy solder attaching and inspection. The pads are all located on the edge of the device so there are no hidden solder joints on these devices. The STM32H7 SOM provides the primary STM32H7-based intelligence on various boards targeting industrial automation, system and power management, wireless networking / sensors and other embedded applications. STM32H7 SOM hardware and software are architected to ensure flexibility in customizing its functionality for the needs of particular products and/or customers.

2. Hardware Platform

This section defines the hardware platform of the STM32H7 SOM.

2.1. Hardware Platform Overview

The following are the key hardware features of the STM32H7 SOM:

- Compact (30.5 mm x 40.5 mm) surface-mount module;
- External interface using 128 castellated edge pads with a 1mm pitch;
- Compliant with the Restriction of Hazardous Substances (RoHS) directive;
- STM32H750 MCU in TFBGA-240 package capable of running the system clock at up to 480 MHz;
- ARM SWJ-DP: a combined JTAG and serial wire debug port;
- 10-pad footprint for TC2050-IDC-NL 10-Pin Plug-of-Nails™ No-Legs Tag-Connect™ Cable for programming and debug;
- Optional 0.05” 20-pin ARM CoreSight connector;
- Powered from single +3.3 V power supply;
- Low-power mode with short startup times;
- Deep-sleep power mode with ultra-low power consumption profiles;
- On-module clocks;
- 32/64 MBytes SDRAM on the 16bit/32bit bus;
- 64 MBytes NOR OSPI Flash;
- Serial console interface at UART CMOS levels;
- 10/100Mbit Ethernet RMII;
- USB 2.0 full-speed device/host/OTG controller with on-chip PHY;
- USB 2.0 high-speed device/host/OTG controller with on-chip ULPI;
- Watchdog Timer (WDT);
- Real-Time Clock (RTC);

- Optional 64kB EEPROM;
- Optional LED driven by a MCU GPO for debug purposes;
- All otherwise uncommitted interfaces of the STM32H7 MCU available on the interface connectors.

2.2. Functional Block Diagram

The following figure is a functional block diagram of the STM32H7 SOM:

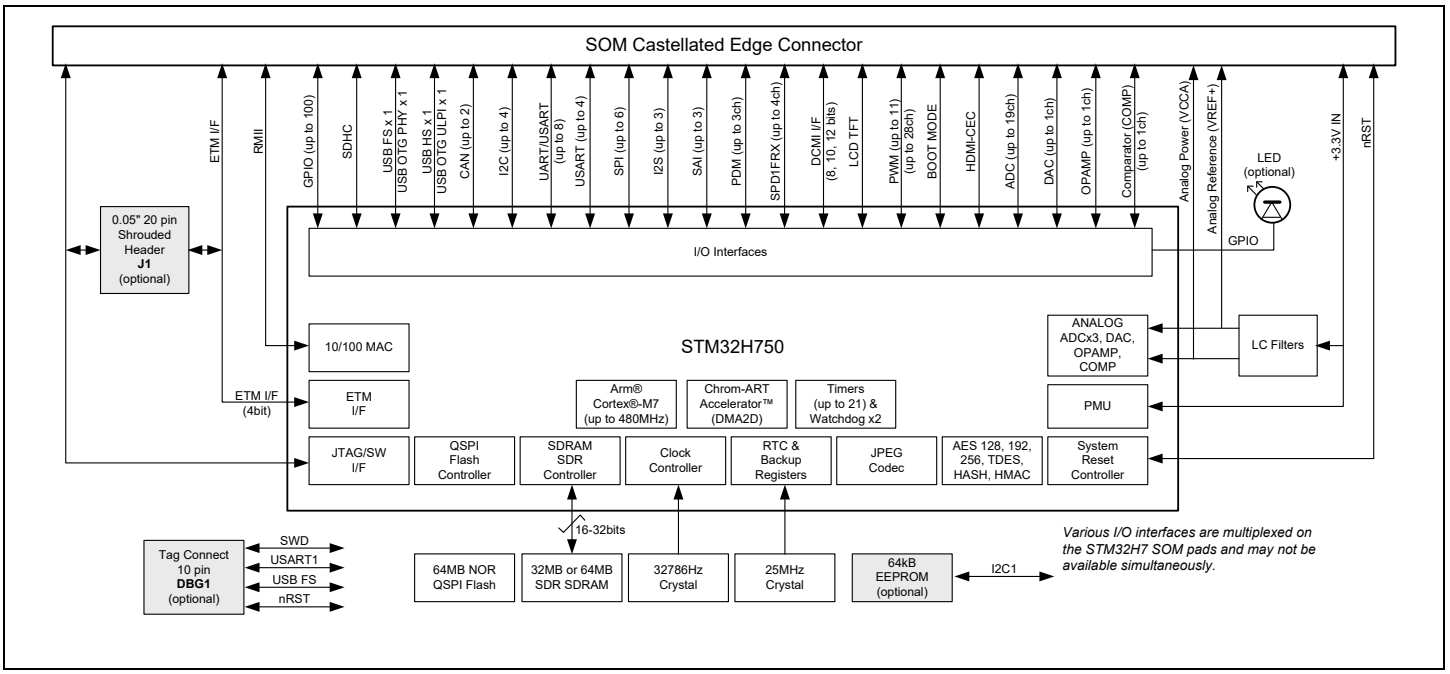

Figure 1: STM32H7 SOM Functional Block Diagram

2.3. Microcontroller

2.3.1. STM32H7 MCU

The architecture of the STM32H7 SOM is built around the STMicro STM32H750 MCU that combines a 32-bit ARM Cortex-M7 processor core with a wide range of the integrated peripheral controllers.

2.4. JTAG/SWD and ETM Interfaces

The Cortex-M7 core supports debugging using real-time traces via the ETM interface as well as debugging via the JTAG/SWD interface. The STM32H7 provides an internal 40kΩ pull-down resistor on the JTCK/SWCLK signal and 40kΩ pull-up resistors on the following signals: JTDI, JTMS/SWDAT, and JTRST after reset.

The STM32H7 SOM provides a standard JTAG/SWD interface on the interface pads and on optional SOM connector. The SWD interface is available also on the SOM TAG connector. These interfaces are routed to the corresponding signals of the STM32H7 device.

The STM32H7 SOM provides an ETM interface with a 4-bit data port on the optional on-SOM connector and on the interface pads. The ETM interface shares pins with the SAI1/SAI4/SPI4 (refer to the STM32H7-SOM-pinout.xlsx file available from the Emcraft web site.)

2.4.1. TAG-Connect™ Pin-Out

The Tag-connect provides SWD, USART and USB interfaces for debug, control, and monitoring the MCU. Table 1 provides TAG-connect connector DBG1 pin-out details.

Pin	Signal Name	Description
1	VCC3	+3.3V SOM power supply
2	NRST	System reset
3	SWCLK/JTCK	Serial wire clock/JTAG test clock
4	SWDIO/JTMS	Serial wire data in/out//JTAG test mode select
5	USART1_TX	USART1 Transmit data
6	USART1_RX	USART1 Receive data
7	USB_FS1_VBUS	USB FS OTG port 1 VBUS input
8	USB_FS1_DM	USB FS OTG port 1 data - line
9	USB_FS1_DP	USB FS OTG port 1 data + line
10	GND	SOM ground

Table 1: TAG-Connect Pad Assignment

2.4.2. ARM CoreSight 20-pin Connector Pin-Out

J1 provides a standard ARM CoreSight 20-pin pin-out. Table 2 provides ARM CoreSight connector pin-out details.

Pin	Signal Name	Description
1	VCC3	+3.3V SOM power supply
2	JTMS	JTAG test mode select/Serial wire data in/out
3	GND	SOM ground
4	JTCK	JTAG test clock/ Serial wire clock
5	GND	SOM ground
6	JTDO	JTAG test data output
7	NA	No pin: KEY
8	JTDI	JTAG test data input
9	GND	SOM ground
10	NRST	System reset
11	NA	No connect
12	TRACE_CK	Trace clock

Pin	Signal Name	Description
13	NA	No connect
14	TRACE0	Trace synchronous data out 0
15	GND	SOM ground
16	TRACE1	Trace synchronous data out 1
17	GND	SOM ground
18	TRACE2	Trace synchronous data out 2
19	GND	SOM ground
20	TRACE3	Trace synchronous data out 3

Table 2: J1 ARM CoreSight Connector Pin Assignment

2.5. Power

2.5.1. Power Source

The STM32H7 SOM is powered from a single +3.3 V power source provided through multiple pins of the interface pads.

2.5.2. MCU Power and I/O Port Voltage Levels

The STM32H750 MCU in the SOM is supplied from the 3.3V input power rail.

The brief data on MCU I/O port levels at the 3.3V power supply (due to the ST specifications) are as follows:

- High and low output levels (@8mA loads) are 3.1V minimum and 0.4V maximum respectively;
- High and low input levels are 1.8V minimum and 0.99V maximum respectively.

Refer to the section "I/O port characteristics" in the STM32H750 datasheet for additional details (available at https://www.st.com/resource/en/datasheet/stm32h750xb.pdf.)

2.5.3. Power Modes

The STM32H7 SOM supports the following power modes:

- Full-power mode. This is the normal mode of operation. The main clock is running and the Cortex-M7 is active running RTOS and/or application code. All memory controllers are enabled.

  The software is configured to enable only those STM32H7 sub-systems that are used by the installed device drivers; all other sub-systems are in reset and do not consume power. When the software doesn't use the external Flash the Flash device is automatically switched to a low power mode (refer to section **Error! Reference source not found.**).

- Low-power mode. The software may be configured to enter this mode of operation when the STM32H7 SOM is idle from the software perspective. The STM32H7 MCU supports three low-power modes: Sleep mode, Stop mode, and Standby mode. Standby mode is used to achieve the lowest power consumption, but all embedded SRAM data and value of all internal registers (except backup domain registers) are lost in this mode. Stop mode achieves the lowest power consumption while retaining the contents of the embedded SRAM and internal registers.

2.6. System Reset

2.6.1. Reset Architecture Overview

The STM32H7 SOM implements a reset architecture that ensures that the STM32H7 MCU is reset as appropriate on various hardware and software events.

Those off-module devices that require synchronization of their resets with the reset of the STM32H7 SOM should have their reset inputs connected to the bidirectional active-low `nRST` signal of the STM32H7 SOM, which is available on pin/pad 30 of the TOP side of the interface connector.

This pin/signal also can be used as an input signal to reset the MCU.

2.6.2. Types of System Resets

The following types of reset are implemented in the STM32H7 SOM:

- Power-on reset (POR). This type of reset occurs when the STM32H7 SOM is being powered-up. The POR threshold is in a range of 1.62V to 1.71.
- Power down reset (PDR). This type of reset occurs when the +3.3V power supply of the STM32H7 SOM falls below the PDR threshold which value is in the range of 1.58V to 1.68V. The hysteresis between the POR and PDR threshold values of a specific STM32H7 chip is 40mV.
- Brown-out reset (BOR). In case when the +3.3 V power supply falls below a user-selectable threshold value (3 regions in the range from 2.05V to 2.78V are available) the BOR system generates a reset of the STM32H7 MCU. After the brown-out reset has occurred, the BOR system holds the STM32H7 MCU in reset until the supply voltage will rise 100mV above the current brownout threshold value.
- Software reset. This type of reset is activated by the software running on the STM32H4 SOM using the STM32H7 software reset sequence.
- WDT reset. This type of reset is activated when the integrated WDT of the STM32H7 MCU expires.
- Manual reset. To activate this type of reset, a baseboard drives low the `nRST` signal of the STM32H7 SOM which is available on pin 30 of the TOP side of the interface connector. This signal/pin mustn’t be actively driven high any time.

2.7. System Clocks

The STM32H7 SOM provides a 25 MHz crystal resonator as a reference to the internal HSE oscillator of the STM32H7 MCU.

After the power-on reset the 64MHz internal HSI RC oscillator is selected as a default CPU clock. After that, the software reconfigures internal clocks of the STM32H7 MCU.

The STM32H7 MCU contains integrated PLLs driven by the internal HSE oscillator, from which various clocks required by subsystems of the STM32H7 MCU are derived.

2.8. SDRAM

2.8.1. SDRAM Architecture

The STM32H7 SOM provides 32/64 MBytes of 166 MHz 16-bit/32-bit SDRAM memory using the one Alliance AS4C16M16SA-6BIN device for 32 Mbytes SDRAM on the 16-bit bus and the two such devices on the 32-bit bus for 64 MBytes SDRAM. The SDRAM memory resides at chip select `FMC_SDNE1` of the integrated Flexible Memory Controller (FMC) of the STM32H7 MCU.

2.8.2. SDRAM Operational Mode

The STM32H7 Flexible Memory controller operates the SDRAM with the SDRAM clock of 100 MHz (HCLK/2) and Burst length = 8.

2.8.3. SDRAM Self Refresh Mode

When in a Self Refresh Mode, the SDRAM current consumption is is 2 mA.

2.9. Flash Memory Architecture

NOR Flash memory chip can be connected to the STM32H7 QSPI bus.

2.9.1. NOR Flash Architecture

The STM32H7 SOM provides 32 MBytes of the NOR Flash memory, using the Micron MT25QL512ABB1EW9-0SIT device. The NOR Flash memory resides at chip select `QUADSPI_BK1_NCS` of Quad-SPI memory interface of the STM32H7 MCU.

2.9.2. NOR Flash Low-Power Mode

When not accessed, the NOR Flash current consumption is only 100 uA.

2.10. Boot Configuration

An STM32H7 boot configuration is set by a state of pin `BOOT0` after the STM32H7 MCU reset. The levels on the `BOOT` pins are latched on the 4th rising edge of `SYSCLK` after the reset. In the STM32H7 SOM the `BOOT0` pin is pulled to the ground by a 10kΩ resistor, so the CPU boots from the integrated Flash memory. BOOT0 is available on TOP Side pin/pad 19, so customer can select booting from the System bootloader by connecting the BOOT0 signal to VCC3 via a 0…1kΩ resistor.

2.11. Serial

2.11.1. UART Controller

The STM32H7 SOM provides an UART serial interface at CMOS levels (no RS-232 buffer) on the interface connectors using the integrated USART1 controller of the STM32H7 MCU.

This interface is intended as a serial console for the U-Boot and uLinux software.

2.12. Ethernet

The STM32H7 SOM provides the 10/100Mbit Ethernet RMII interface on the SOM pads for an external off-module RMII Ethernet PHY.

2.13. WDT

The STM32H7 SOM provides a hardware watchdog function using two embedded WDT peripherals: Independent and Window. The independent watchdog (IWDG) is clocked by its own dedicated low-speed clock (LSI) and therefore stays active even if the main clock fails. The window watchdog (WWDG) clock is prescaled from the APB clock and has a configurable time-window that can be programmed to detect abnormally late or early application behavior.

If the WDT is enabled and the software fails to strobe the WDT within the predefined period of time, the watchdog triggers reset.

The WDT timeout period is defined by the software.

2.14. RTC

The STM32H7 SOM supports a Real-Time Clock (RTC) functionality using the Real-Time Counter System of the STM32H7 MCU.

The RTC clock source is the low-power 32.768 KHz oscillator of the STM32H7 MCU.

The battery switching circuitry continuously compares the battery voltage (the `VBAT` signal on the interface connector) with the voltage of the main digital power supply (the `VDD` pins of the STM32H7 MCU) and automatically powers the RTC and the 32.768 KHz oscillator from the battery whenever the battery voltage is approximately 0.6 V or more, above the voltage on the `VDD` pin. This allows both the RTC and the 32.768 KHz oscillator to function when the +3.3V power supply is removed.

2.15. User Interface LED Indicator

System Status LED HL1 (optional) has the following functions:

- Green blinking – CPU is running well;
- OFF - CPU is not running.

HL1 is driven by STM32H7 GPIO `PI8` via a 270Ω resistor.

2.16. External Interface

2.16.1. Interface Connectors

The external interfaces of the STM32H7 SOM are routed through 128 castellated edge pads with the 1mm pitch.

2.16.2. Connectors Pin-Out

Refer to the STM32H7-SOM-pinout.xlsx file available from the Emcraft web site for the detailed information on connectors pin-out.

2.16.3. Unavailable Signals of STM32H7

In the STM32H7 SOM all signals of the STM32H7 MCU are either used in the memory interfaces or connected to the interface connectors. The memory interface signals are not available on the interface connectors.

3. Mechanical Specifications

3.1. STM32H7 SOM Mechanicals

The STM32H7 SOM is implemented as a miniature 30.5 mm x 40.5 mm x 2.8 mm module.

The STM32H7 SOM PCB thickness is 1.6 mm +/- 0.16 mm. The maximum height of the SOM components is 1.2 mm without the optional 20-pin ARM CoreSight connector. The height of the 20-pin ARM CoreSight connector is 5.6mm.

The following figure shows locations of the mounting hole and the SOM connectors on the module:

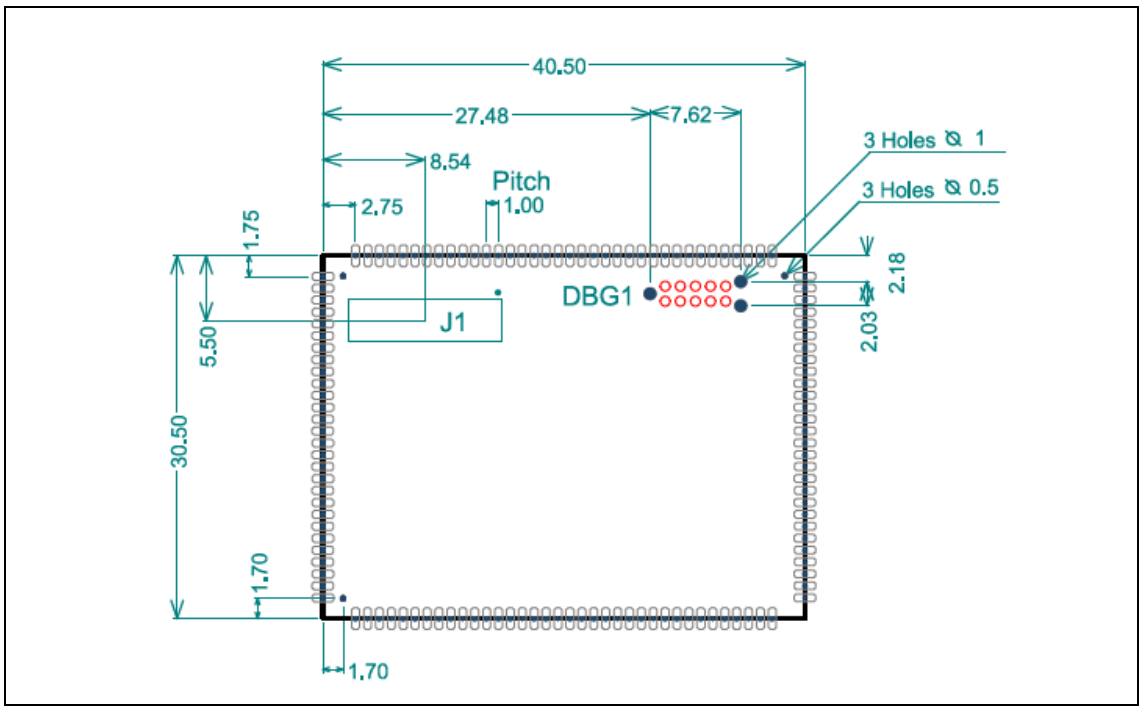

Figure 2: STM32H7 SOM Top View

3.2. STM32H7 SOM Footprint

The STM32H7 SOM is a surface-mount module and it is soldered to the baseboard. The recommended baseboard footprint for the STM32H7-SOM is presented on Figure 3 below.

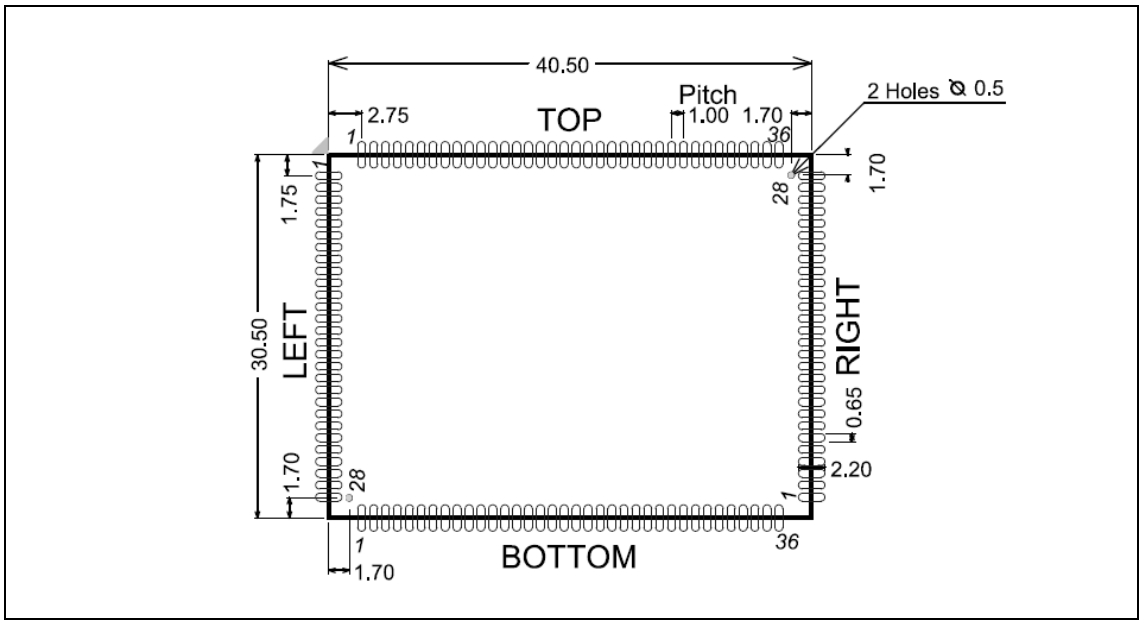

Figure 3: STM32H7 SOM Footprint

3.3. STM32H7 SOM Top and Bottom Views

The following pictures provide the top and bottom views of the STM32H7 SOM:

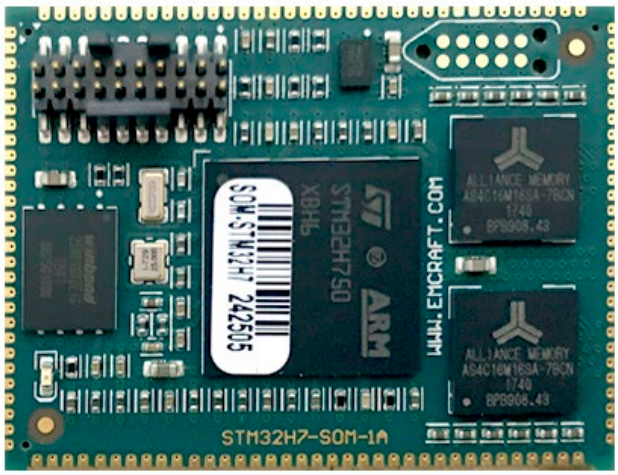

Figure 4: STM32H7 SOM Top View

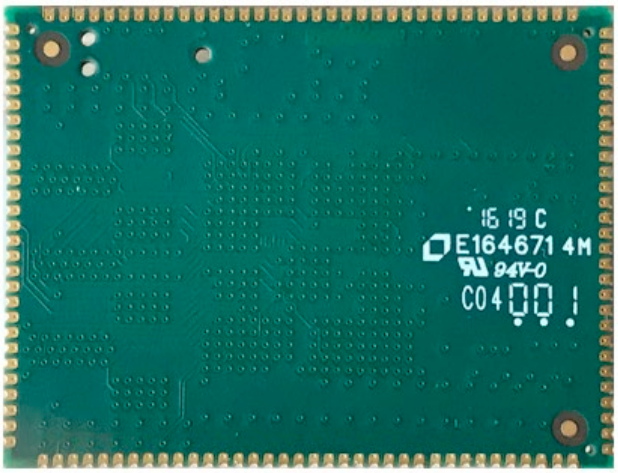

Figure 5: STM32H7 SOM Bottom View

4. Environment Specifications

4.1. Recommended Operating Conditions

The following table lists the recommended operating conditions of the STM32H7 SOM:

Symbol	Parameter	Range
Ta	Ambient temperature	-40 to +85 ºC (Industrial)
VCC3	+3.3 V power supply	+3.3 V +/-5%

Table 5: Recommended Operating Conditions

5. Ordering Specifications

The following table provides the ordering information for the STM32H7 SOM:

Ordering Part Number	Specification
SOM-STM32H7-R[32|64]N64[C|I]	ST STM32H750 32-bit 480MHz ARM Cortex-M7, 32 MB or 64MB SDRAM, 64MB NOR Flash, Commercial or Industrial Temp.

Table 3: Ordering Specifications

6. Document Revision History

Revision	Date	Changes Summary
1.1	April 20, 2023	• Removed 128MB QSPI NAND Flash option.
1.0	March 31, 2021	Initial revision.