# i.MX 8M Mini LPDDR4 System-On-Module (SOM)

## Hardware Architecture

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# 1. Introduction

This document describes the hardware architecture of the Emcraft Systems i.MX 8M Mini LPDDR4 System-on-Module (referred to as "i.MX 8M Mini LPDDR4 SOM" hereafter).

The i.MX 8M Mini LPDDR4 System-On-Module (SOM) is a mezzanine module (50.8mm x 50.8mm) that combines the NXP i.MX 8M Mini multi-core application processor with up to 4GB LPDDR4 SDRAM, up to 64GB eMMC, up to 32MB NOR QSPI Flash memory and a WiFi / Bluetooth module on a single board. The i.MX 8M Mini LPDDR4 SOM features up to four Cortex-A53 cores at 1.8GHz and a Cortex-M4 core for low-power and real-time operation.

# 2. Hardware Platform

This section defines the hardware platform of the i.MX 8M Mini LPDDR4 SOM.

## 2.1. Hardware Platform Overview

The following are the key hardware features of the i.MX 8M Mini LPDDR4 SOM:

- Compact mezzanine module (50.8mm x 50.8mm);
- External interfaces using two 100-pin and one 20-pin 0.4mm-pitch connectors;
- Three mounting holes reducing the risk of connector-to-PCB intermittence;
- Four mounting holes for attaching a heatsink;
- Compliant with the Restriction of Hazardous Substances (RoHS) directive;
- NXP i.MX 8M Mini microprocessor with Quad Cortex-A53 cores at 1.8GHz and a Cortex-M4 core for low-power and real-time operation;
- JTAG interface to the i.MX 8M Mini;
- Embedded Trace Macrocell (ETM);
- Powered from a single +5V power supply;
- Low-power operational modes with fast wake-up;
- 1-4GB LPDDR4 SDRAM;
- 4-64GB eMMC Flash;
- IEEE802.11a/b/g/n/ac W-LAN + Bluetooth 5.0 BR/EDR/LE;
- U.FL connector for WiFi & BT external antennas;
- Serial console interface at the UART CMOS levels;
- 1Gb Ethernet RGMII interface;
- Two USB 2.0 controllers with integrated PHY interfaces;
- PCI Express Gen2 interface;
- MIPI-DSI Display Interface (resolution up to 1920 x 1080 at 60Hz);
- MIPI-CSI2 camera input (4-lane);
- Various digital (UART, SPI, I2C, SDHC, SAI, GPIO) interfaces of the i.MX 8M Mini LPDDR4 SOM available on the interface connectors.

## 2.2. Functional Block Diagram

The following figure is a functional block diagram of the i.MX 8M Mini LPDDR4 SOM:

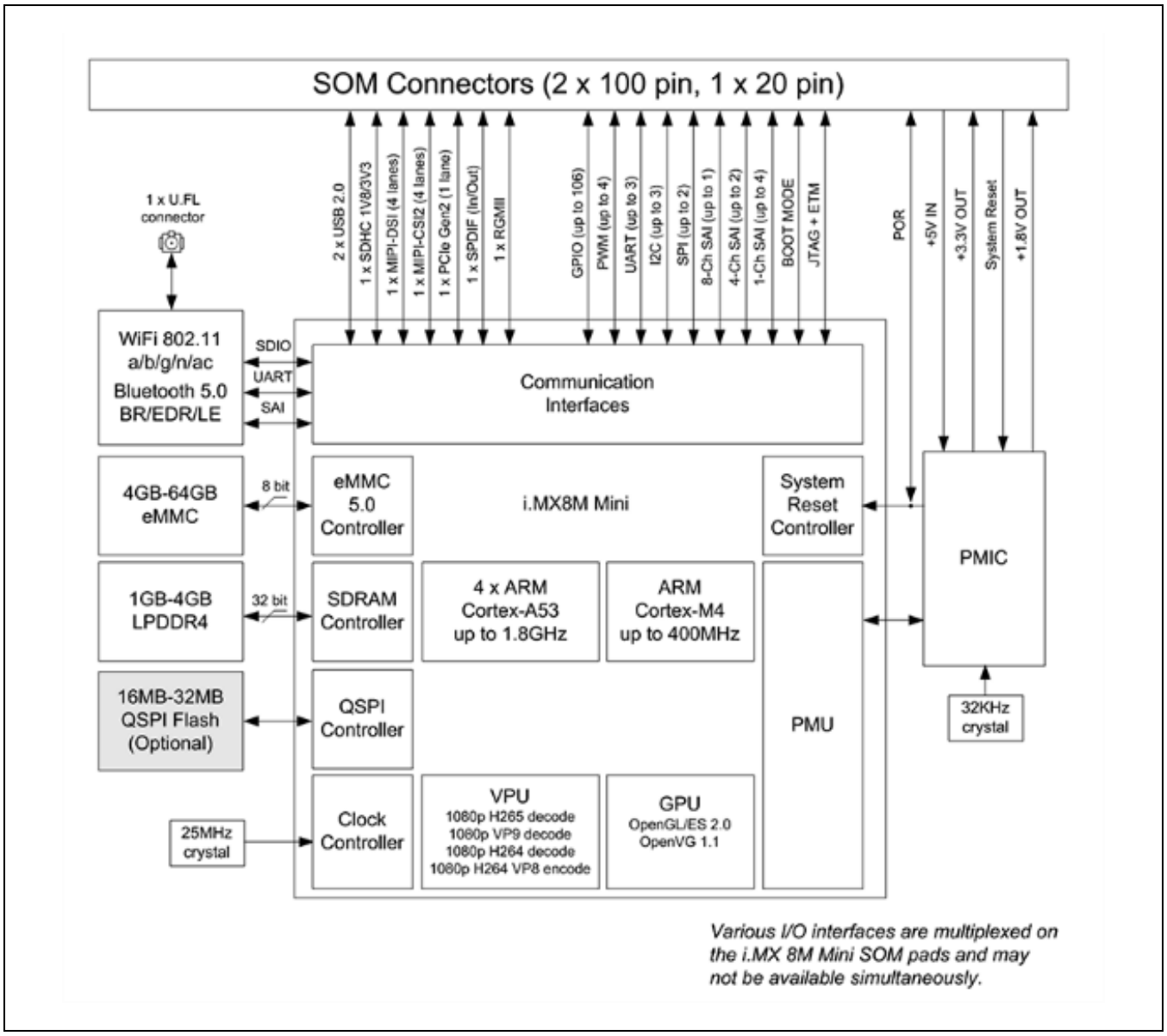


**Figure 1:** i.MX 8M Mini LPDDR4 SOM Functional Block Diagram

## 2.3. Microcontroller

### 2.3.1. Microcontroller Device

The architecture of the i.MX 8M Mini LPDDR4 SOM is built around the NXP i.MX 8M Mini microprocessor that combines the 1.8GHz Quad ARM Cortex-A53 processor cores with a 400MHz Cortex-M4 co-processor core as well as a wide range of the integrated peripheral controllers.

The NXP i.MX 8M Mini device is implemented using the 14mm x 14mm 0.5mm-pitch Map BGA package.

### 2.3.2. Microcontroller Configuration

The i.MX 8M Mini LPDDR4 SOM supports the following NXP i.MX 8M Mini device (SOM build-time options):

- MIMX8MM6DVTLZAA.

### 2.3.3. Microcontroller Boot Selection

The NXP i.MX 8M Mini code is configured to use the on-module eMMC Flash memory as the boot device. This is achieved by using the pre-programmed fuse configuration. The "Boot from Fuses" mode is set by 95kOhm internal pull-down resistors on the NXP i.MX 8M Mini `BOOT0` and `BOOT1` pins.

Note that the above boot pins are also routed to the i.MX 8M Mini LPDDR4 SOM connector J4 (refer to Section 2.12.2). Care must be taken not to override the state of the above pins during boot time on a carrier board, otherwise the NXP i.MX 8M Mini may fail to boot.

## 2.4. JTAG and ETM Interfaces

The Cortex-A53 and Cortex-M4 cores support debugging using real-time traces via the ETM interface as well as debugging via the JTAG interface.

The i.MX 8M Mini LPDDR4 SOM provides a standard JTAG interface on the interface connectors and on-SOM Test Points. This interface is routed to the corresponding signals of the NXP i.MX 8M Mini device. The NXP i.MX 8M Mini provides internal 27k pull-up resistors on the JTAG pins.

The i.MX 8M Mini LPDDR4 SOM provides an ETM interface with a 16-bit data port on the interface connectors. The ETM interface shares pins with the SAI1 (refer to the imx8m-mini-som-pinout.xlsx file available from the Emcraft web site.)

## 2.5. Power

### 2.5.1. Power Source

The i.MX 8M Mini LPDDR4 SOM is powered from a single +5V power source provided through multiple pins on the interface connectors.

The power source should provide at least 2A/10W power for the i.MX 8M Mini LPDDR4 SOM to operate.

The i.MX 8M Mini LPDDR4 SOM 2.54mm 2-pin header J6 (not populated by default) provides the input power rails. Table 1 details the header pin-out.

| Pin | Signal Name | Description |
|---|---|---|
| 1 | `VSYS_5V` | +5V SOM input power supply |
| 2 | `GND` | SOM ground |

**Table 1:** System Power Header Pin Assignment

### 2.5.2. Power Control and Monitoring

Power control and monitoring on the i.MX8M Mini LPDDR4 SOM is implemented using the Rohm Power Control Integrated Circuit (PMIC) BD71847MWV-E2, designed specifically for the NXP i.MX 8M Mini family of application processors.

The BD71847MWV-E2 provides Dynamic Voltage Scaling via I²C bus and/or digital input `PMIC_STBY_REQ`. The PMIC is accessible on the i.MX 8M Mini `I2C1` bus for read and write at addresses 0x97 and 0x96, respectively.

### 2.5.3. Power Modes

The i.MX 8M Mini LPDDR4 SOM supports the following power modes:

- Full-power mode. This is the normal mode of operation. The main clock is running and the Cortex-A53 cores are running Linux. All memory controllers are enabled.

- Software is configured to enable only those NXP i.MX 8M Mini sub-systems that are used by installed device drivers; the clocks to all other sub-systems are gated off so those modules do not consume power.

  Low-power mode. This is Linux low-power mode, also referred to as the "Linux suspend-to-RAM" mode of operation. When Linux is commanded to enter the low-power mode, it transitions the SDRAM device to the self-refresh mode, ensuring that the Linux operational content is preserved across the low-power mode. The on-module WiFi/BT module is put into a low-power mode. The Cortex-A53 cores are put into appropriate low power modes.

  The i.MX 8M Mini LPDDR4 SOM remains in the low-power mode until woken up by a configured trigger (such as, for instance, activation of a configured GPIO). On occurrence of a wake-up trigger, the i.MX 8M Mini LPDDR4 SOM returns to the full-power mode.

## 2.6. System Reset

### 2.6.1. Reset Architecture Overview

The i.MX 8M Mini LPDDR4 SOM implements a reset architecture that ensures that the NXP i.MX 8M Mini microprocessor is reset as appropriate on various hardware and software events.

### 2.6.2. Types of System Resets

The following types of reset are implemented by the i.MX 8M Mini LPDDR4 SOM:

- Power-on reset. This type of reset occurs when the power is initially applied to the i.MX 8M Mini LPDDR4 SOM. As the supply voltage rises, the on-SOM PMIC holds the NXP i.MX 8M Mini in reset until all the processor power supply voltages have risen above the appropriate voltage thresholds (90% of the nominal values). The internal i.MX 8M Mini LPDDR4 SOM power-on reset generation is disabled.
- Brown-out reset. In case any processor supply falls below/rises above its 80%/130% of its nominal voltage level, the PMIC generates a reset of the NXP i.MX 8M Mini. After the brown-out reset has occurred, the PMIC holds the i.MX 8M Mini in reset until all the supplies return to the range 90-110% of their nominal values.
- Software reset. This type of reset is activated by software running on the i.MX 8M Mini LPDDR4 SOM through performing the i.MX 8M Mini LPDDR4 SOM software reset sequence.
- External reset. To activate this type of reset, a baseboard drives low the `SYS_nRST` signal on the i.MX 8M Mini LPDDR4 SOM interface connectors. Activating this signal leads to the i.MX8M Mini LPDDR4 SOM power cycle.

## 2.7. System Clocks

The i.MX 8M Mini LPDDR4 SOM provides 24MHz quartz crystal as the references to the internal oscillators of the NXP i.MX 8M Mini microprocessor.

## 2.8. SDRAM

### 2.8.1. SDRAM Architecture

The i.MX 8M Mini LPDDR4 SOM provides 1-4GB of LPDDR4 SDRAM using one of the following device (build-time option):

- Micron MT53B256M32D1NP-062 WT:C;
- Micron MT53B512M32D2NP-062 WT:C (MT53B512M32D2NP-053 WT:C);
- Micron MT53B1024M32D4NQ-062 WT:C.

### 2.8.2. SDRAM Operational Mode

The i.MX 8M Mini LPDDR4 SOM SDRAM controller operates in the LPDDR4 mode. The DDR clock frequency of the SDRAM controller is 1500MHz.

## 2.9. eMMC

### 2.9.1. eMMC Architecture

The i.MX 8M Mini LPDDR4 SOM provides 4-64GB of eMMC Flash interface using one of the following the devices (build-time option):

- Kingston EMMC04G-M627-X02U;
- Western Digital SDINBDG4-8G-I1;
- Western Digital SDINBDG4-16G-I1;
- Western Digital SDINBDG4-32G-I1;
- Western Digital SDINBDG4-64G-I1.

### 2.9.2. eMMC Operational Mode

The eMMC Flash operates in an 8-bit mode.

## 2.10. WiFi and Bluetooth

### 2.10.1. Wireless Architecture

The i.MX 8M Mini LPDDR4 SOM provides 802.11a/b/g/n/ac WLAN and Bluetooth 5.0 BR/EDR/LE functions. This is implemented with the Murata LBEE5HY1MW-230 module which is based on the Cypress CYW43455 chipset.

#### 2.10.1.1 WiFi

The W-LAN interface is supported via i.MX 8M Mini LPDDR4 SOM SD port 1.

#### 2.10.1.2 Bluetooth

Bluetooth is supported via the i.MX 8M Mini LPDDR4 SOM UART1 (data path). The UART3 data path pins (`TXD` and `RXD`) are used as a UART1 flow control.

The Bluetooth digital audio is provided with the i.MX 8M Mini LPDDR4 SOM SAI2 (in the PCM mode).

### 2.10.2. WiFi & BT Connectors

The i.MX8M Mini LPDDR4 SOM provides one U.FL connector (J2) for external WiFi/BT antenna.

The Molex 1461530100 antenna is recommended for using with the i.MX8M Mini LPDDR4 SOM.

The placeholders L3, L4, R44 are reserved on the i.MX8M Mini LPDDR4 SOM for external antennas matching circuits. By default, only 0-Ohm R44 is installed.

## 2.11. User Interface LED Indicator

System Status LED D1 has the following functions:

- Green blinking – CPU is running well;
- OFF - CPU is not running.

D1 is driven by i.MX8M Mini LPDDR4 SOM `GPIO3_IO16` (CPU pad `NAND_READY_B`) via a MOSFET buffer.

## 2.12. External Interface

### 2.12.1. Board to Board Interface Connectors

The external interfaces of the i.MX 8M Mini LPDDR4 SOM are routed through two 100-pin and one 20-pin Hirose DF40 series 0.4mm-pitch board-to-board connectors.

### 2.12.2. Connectors Pin-Out

Refer to the imx8m-mini-som-pinout.xlsx file available from the Emcraft web site for the detailed information on connectors pin-out.

# 3. Mechanical Specifications

## 3.1. i.MX 8M Mini LPDDR4 SOM Mechanicals

The i.MX 8M Mini LPDDR4 SOM is implemented as a 50.8mm x 50.8mm x 3.7mm module (without a processor heatsink and the bottom side connectors).

The i.MX 8M Mini LPDDR4 SOM PCB thickness is 1.2±0.12mm. The maximum height of the SOM components on the top and bottom sides of the module is 1.25mm and 1.1mm respectively.

The i.MX 8M Mini LPDDR4 SOM includes three 2.77mm mounting holes for fastening the SOM to a baseboard, four 1.63mm mounting holes for attaching, and two 0.89mm holes for polarizing a heatsink to the i.MX8M package.

The following figure shows the location of the mounting holes and the SOM connectors on the module:

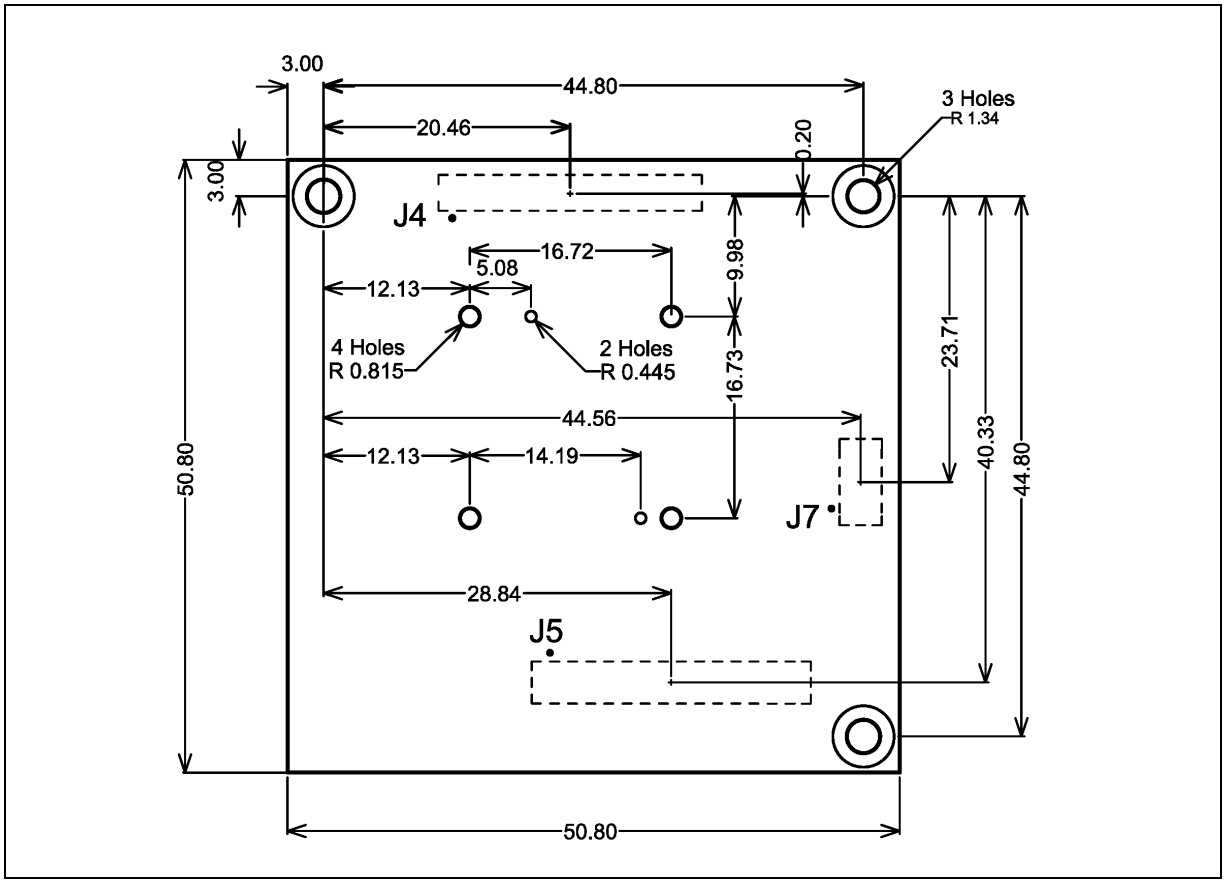


**Figure 2:** i.MX 8M Mini LPDDR4 SOM Top View

Connectors J4, J5, and J7 are on the bottom side. All dimensions are in millimeters.

## 3.2. i.MX 8M Mini LPDDR4 SOM Connectors Mechanicals

On a baseboard, the i.MX 8M Mini LPDDR4 SOM is installed into two 100-pin and one 20-pin Hirose DF40 series 0.4mm-pitch board-to-board connectors. The exact part number of the connectors J4, J5, and J7 are Hirose DF40C-100DP-0.4V(51), DF40C-100DS-0.4V(51), and DF40C-20DS-0.4V(51) respectively.

The recommended mating connectors for a baseboard is the Hirose DF40C-100DS-0.4V(51), DF40C-100DP-0.4V(51) and DF40C-20DP-0.4V(51) connectors, which provides 1.5mm stacking height for the i.MX 8M Mini LPDDR4 SOM. The maximum height of the SOM above a baseboard for 1.5mm stacking height is 4.1mm without a processor heatsink.

## 3.3. i.MX 8M Mini LPDDR4 SOM Top and Bottom Views

The following pictures provide the top and bottom views of the i.MX 8M Mini LPDDR4 SOM:


**Figure 3:** i.MX 8M Mini LPDDR4 SOM Top View

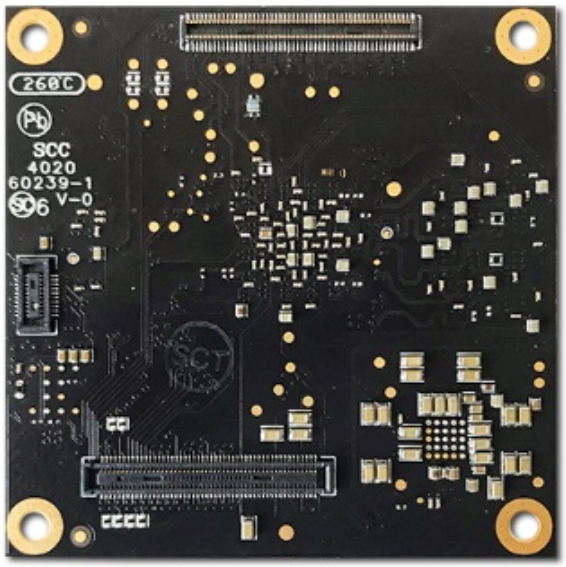


**Figure 4:** i.MX 8M Mini LPDDR4 SOM Bottom View

# 4. Environment Specifications

## 4.1. Recommended Operating Conditions

The following table lists the recommended operating conditions of the i.MX 8M Mini LPDDR4 SOM:

| Symbol | Parameter | Range | |
|---|---|---|---|
| $T_A$ | Ambient temperature | Commercial | 0 to +70 ºC |
| SYS_5V | +5V power supply | +5V +/-5% | |

**Table 2:** Recommended Operating Conditions

# 5. Document Revision History

| Revision | Date | Changes Summary |
|---|---|---|
| 1.0 | January 27, 2021 | Initial version |