i.MX 8M Plus System-On-Module (SOM)

Hardware Architecture

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1. Introduction

This document describes the hardware architecture of the Emcraft Systems i.MX 8M Plus System-on-Module (referred to as "i.MX 8M Plus SOM" hereafter).

The i.MX 8M Plus System-On-Module (SOM) is a mezzanine module (58.4mm x 58.4mm) that combines the NXP i.MX 8M Plus multi-core application processor with up to 8GB LPDDR4 SDRAM, 32GB eMMC, up to 32MB NOR QSPI Flash memory. The i.MX 8M Plus SOM features up to four Cortex-A53 cores at 1.8GHz and a Cortex-M7 core at 800MHz for low-power and real-time operation.

2. Hardware Platform

This section defines the hardware platform of the i.MX 8M Plus SOM.

2.1. Hardware Platform Overview

The following are the key hardware features of the i.MX 8M Plus SOM:

- Compact mezzanine module (58.4mm x 58.4mm);
- External interfaces using four 100-pin 0.4mm-pitch connectors;
- Three mounting holes reducing the risk of connector-to-PCB intermittence;
- Compliant with the Restriction of Hazardous Substances (RoHS) directive;
- NXP i.MX 8M Plus microprocessor with Quad Cortex-A53 cores at 1.8GHz and a Cortex-M7 at 800MHz core for low-power and real-time operation;
- Machine Learning Neural Processor Unit (NPU);
- Image Sensor Processor (ISP);
- JTAG interface to the i.MX 8M Plus;
- Powered from a single +5V power supply;
- Low-power operational modes with fast wake-up;
- 4-8GB LPDDR4 SDRAM;
- 32GB eMMC Flash;
- Serial console interface at the UART CMOS levels;
- 1Gb Ethernet RGMII interface;
- Two USB 2.0 controllers with integrated PHY interfaces;
- Two USB 3.0 controllers with integrated PHY interfaces;
- PCI Express Gen2 interface;
- MIPI-DSI Display Interface (resolution up to 2560 x 1080 at 60Hz);
- Two MIPI-CSI2 camera input (4-lane);
- Two LVDS Display interfaces (4-lane);
- HDMI 2.0a interface (resolution up to 3840 x 2160 at 30Hz);
- Various digital (UART, SPI, I2C, SDHC, SAI, CAN, SPDIF, PDM, GPIO) interfaces of the i.MX 8M Plus SOM available on the interface connectors.

2.2. Functional Block Diagram

The following figure is a functional block diagram of the i.MX 8M Plus SOM:

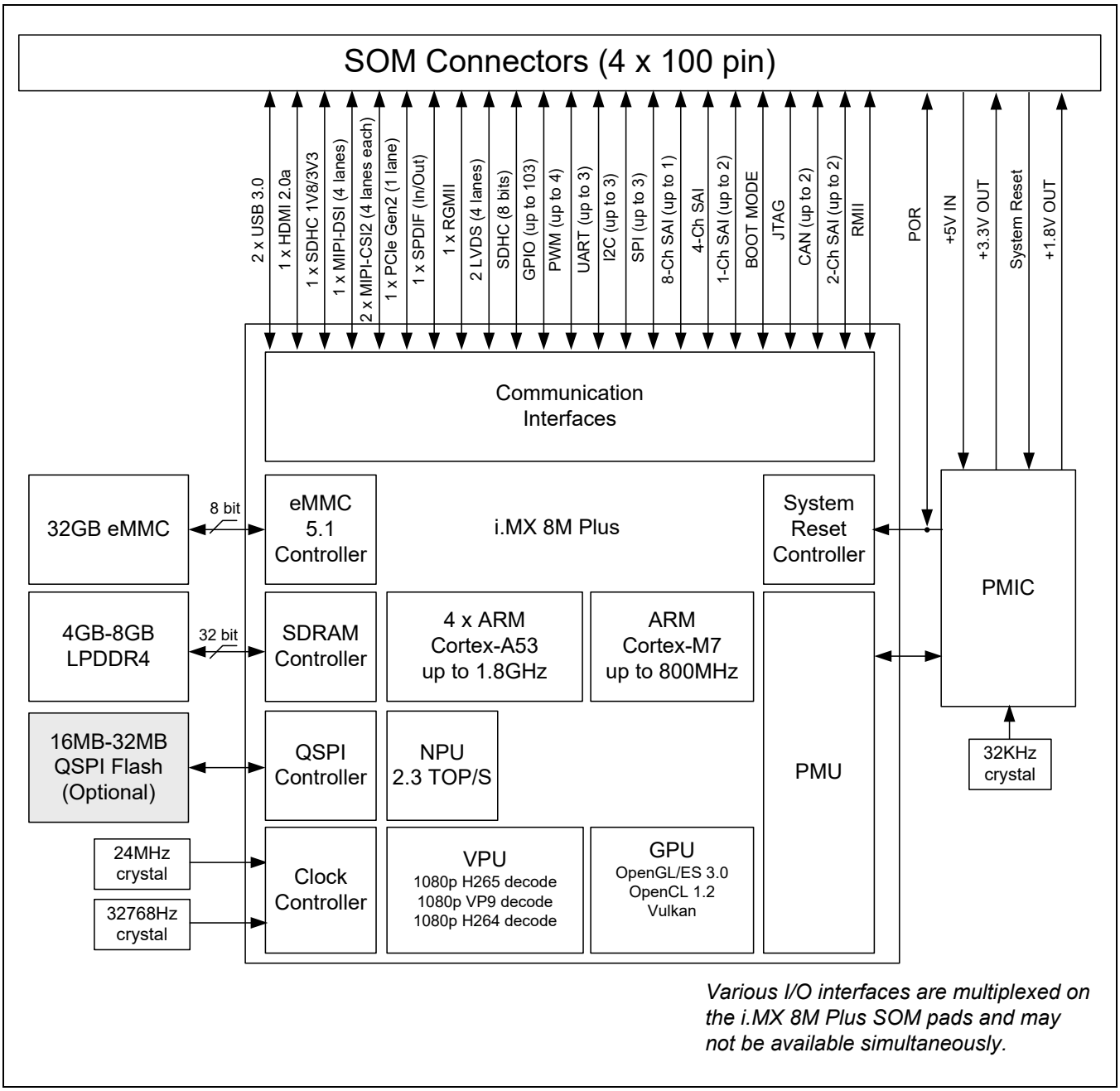

Figure 1: i.MX 8M Plus SOM Functional Block Diagram

2.3. Microcontroller

2.3.1. Microcontroller Device

The architecture of the i.MX 8M Plus SOM is built around the NXP i.MX 8M Plus microprocessor that combines the 1.8GHz Quad ARM Cortex-A53 processor cores with a 400MHz Cortex-M7 co-processor core as well as a wide range of the integrated peripheral controllers.

The NXP i.MX 8M Plus device is implemented using the 15mm x 15mm 0.5mm-pitch Map BGA package.

2.3.2. Microcontroller Configuration

The i.MX 8M Plus SOM supports the following NXP i.MX 8M Plus device (SOM build-time options):

- MIMX8ML8DVNLZAA.

2.3.3. Microcontroller Boot Selection

The NXP i.MX 8M Plus code is configured to use the on-module eMMC Flash memory as the boot device. This is achieved by using the pre-programmed fuse configuration. The "Boot from Fuses" mode is set by 43kOhm internal pull-down resistors on the NXP i.MX 8M Plus `BOOT_MODE[3..0]` pins.

Note that the above boot pins are also routed to the i.MX 8M Plus SOM connector J3 (refer to Section 2.12.2). Care must be taken not to override the state of the above pins during boot time on a carrier board, otherwise the NXP i.MX 8M Plus may fail to boot.

2.4. JTAG Interface

The Cortex-A53 and Cortex-M7 cores support debugging via the JTAG interface.

The i.MX 8M Plus SOM provides a standard JTAG interface on the interface connectors and on-SOM Test Points. This interface is routed to the corresponding signals of the NXP i.MX 8M Plus device. The NXP i.MX 8M Plus provides internal 37k pull-up resistors on the JTAG pins.

2.5. Power

2.5.1. Power Source

The i.MX 8M Plus SOM is powered from a single +5V power source provided through multiple pins on the interface connectors.

The power source should provide at least 2A/10W power for the i.MX 8M Plus SOM to operate.

2.5.2. Power Control and Monitoring

Power control and monitoring on the i.MX8M Plus SOM is implemented using the NXP Power Control Integrated Circuit (PMIC) PCA9450CHN, designed specifically for the NXP i.MX 8M Plus family of application processors.

The PCA9450CHN provides Dynamic Voltage Scaling via I²C bus and/or digital input `PMIC_STBY_REQ`. The PMIC is accessible on the i.MX 8M Plus `I2C1` bus for read and write at addresses 0x4b and 0x4a, respectively.

2.5.3. Power Modes

The i.MX 8M Plus SOM supports the following power modes:

- Full-power mode. This is the normal mode of operation. The main clock is running and the Cortex-A53 cores are running Linux. All memory controllers are enabled.
- Software is configured to enable only those NXP i.MX 8M Plus sub-systems that are used by installed device drivers; the clocks to all other sub-systems are gated off so those modules do not consume power.

  Low-power mode. This is Linux low-power mode, also referred to as the "Linux suspend-to-RAM" mode of operation. When Linux is commanded to enter the low-power mode, it transitions the SDRAM device to the self-refresh mode, ensuring that the Linux operational content is preserved across the low-power mode. The Cortex-A53 cores are put into appropriate low power modes.

  The i.MX 8M Plus SOM remains in the low-power mode until woken up by a configured trigger (such as, for instance, activation of a configured GPIO). On occurrence of a wake-up trigger, the i.MX 8M Plus SOM returns to the full-power mode.

2.6. System Reset

2.6.1. Reset Architecture Overview

The i.MX 8M Plus SOM implements a reset architecture that ensures that the NXP i.MX 8M Plus microprocessor is reset as appropriate on various hardware and software events.

2.6.2. Types of System Resets

The following types of reset are implemented by the i.MX 8M Plus SOM:

- Power-on reset. This type of reset occurs when the power is initially applied to the i.MX 8M Plus SOM. As the supply voltage rises, the on-SOM PMIC holds the NXP i.MX 8M Plus in reset until all the processor power supply voltages have risen above the appropriate voltage thresholds (90% of the nominal values). The internal i.MX 8M Plus SOM power-on reset generation is disabled.
- Brown-out reset. In case any processor supply falls below its 85% of its nominal voltage level, the PMIC generates a reset of the NXP i.MX 8M Plus. After the brown-out reset has occurred, the PMIC holds the i.MX 8M Plus in reset until all the supplies return to a value above 85% of their nominal values.
- Software reset. This type of reset is activated by software running on the i.MX 8M Plus SOM through performing the i.MX 8M Plus SOM software reset sequence.
- External reset. To activate this type of reset, a baseboard drives low the `SYS_nRST` signal on the i.MX 8M Plus SOM interface connectors. Activating this signal leads to the i.MX8M Plus SOM power cycle.

2.7. System Clocks

The i.MX 8M Plus SOM provides 24MHz quartz crystal as the references to the internal oscillators of the NXP i.MX 8M Plus microprocessor.

2.8. SDRAM

2.8.1. SDRAM Architecture

The i.MX 8M Plus SOM provides 2-8GB of LPDDR4 SDRAM using one of the following device (build-time option):

- Kingston Q3222PM1WDGTK-U;
- Micron MT53E1G32D2NP-046WT:B;
- Micron MT53E2G32D4NP-046WT:B.

2.8.2. SDRAM Operational Mode

The i.MX 8M Plus SOM SDRAM controller operates in the LPDDR4 mode. The DDR clock frequency of the SDRAM controller is up to 2000MHz (may be variated by the Dynamic Voltage and Frequency Scaling block of the i.MX8M Plus processor).

2.9. eMMC

2.9.1. eMMC Architecture

The i.MX 8M Plus SOM provides 32GB of eMMC Flash interface using one of the following the device:

- Kingston EMMC32G-IB29-90F01

2.10. RTC

The i.MX 8M Plus SOM provides a hardware RTC (Real-Time Counter) using the integrated SNVS_LP RTC of the i.MX 8M Plus. The i.MX 8M Plus SNVS_LP RTC has the following main features:

- The SNVS_LP RTC provides a programmable time alarm interrupt which can be used only for wake-up from the shutdown (power-off) state if the SNVS power supplies are active.

The RTC uses an 32kHz external crystal as a clock reference.

2.11. User Interface LED Indicator

System Status LED D1 has the following functions:

- Green blinking – CPU is running well;
- OFF - CPU is not running.

D1 is driven by i.MX8M Plus SOM GPIO3_IO16 (CPU pad NAND_READY_B) via a MOSFET buffer.

2.12. External Interface

2.12.1. Board to Board Interface Connectors

The external interfaces of the i.MX 8M Plus SOM are routed through four 100-pin Hirose DF40 series 0.4mm-pitch board-to-board connectors.

2.12.2. Connectors Pin-Out

Refer to the imx8m-plus-som-pinout.xlsx file available from the Emcraft web site for the detailed information on connectors pin-out.

3. Mechanical Specifications

3.1. i.MX 8M Plus SOM Mechanicals

The i.MX 8M Plus SOM is implemented as a 58.4mm x 58.4mm x 3.7mm module (without a processor heatsink and the bottom side connectors).

The i.MX 8M Plus SOM PCB thickness is 1.2±0.12mm. The maximum height of the SOM components on the top and bottom sides of the module is 1.48mm and 1.0mm, respectively.

The i.MX 8M Plus SOM includes three 2.8mm mounting holes for fastening the SOM to a baseboard.

The following figure shows the location of the mounting holes and the SOM connectors on the module:

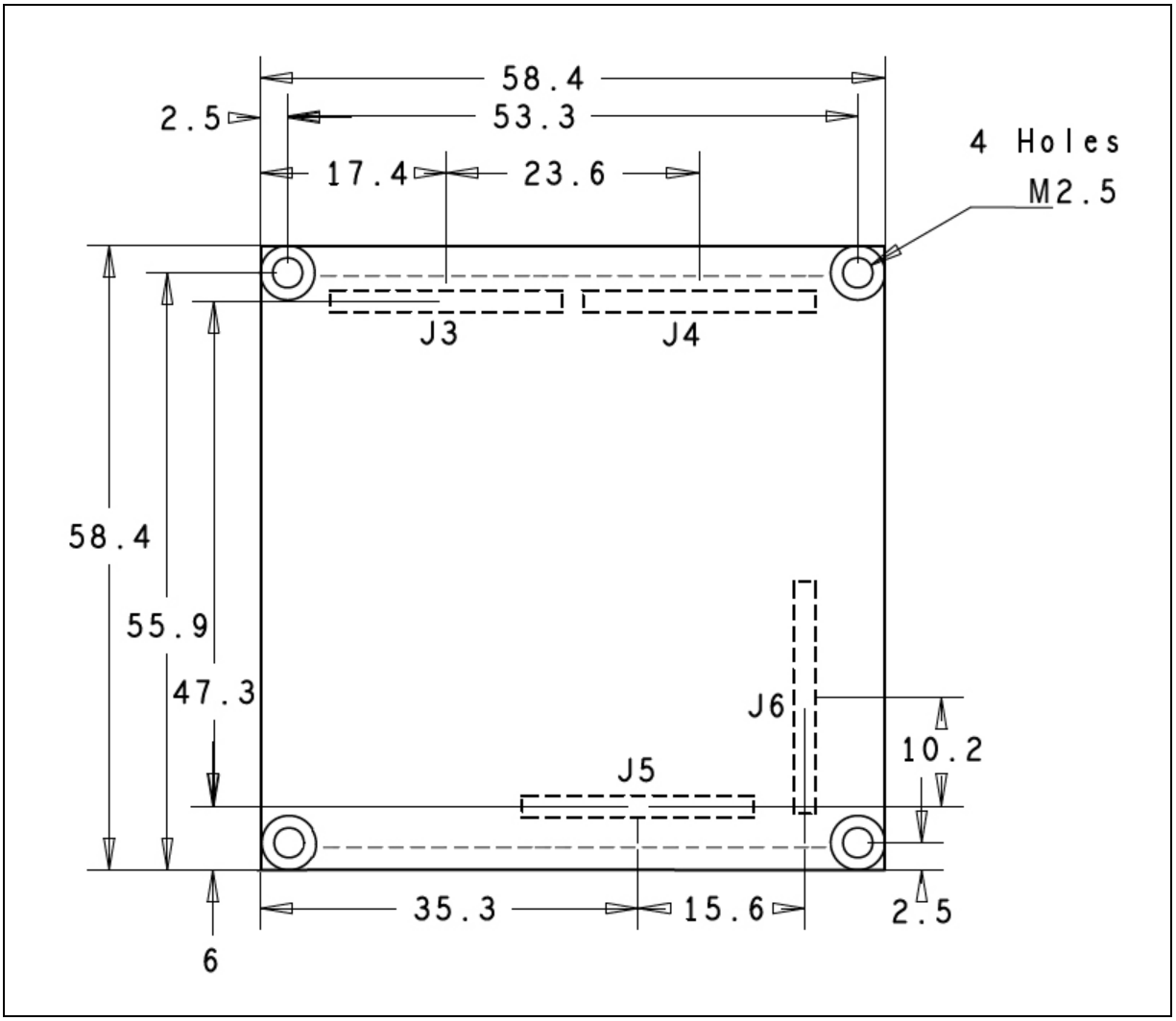

Figure 2: i.MX 8M Plus SOM Mechanical Drawing

Connectors J3, J4, J5, and J6 are on the bottom side. All dimensions are in millimeters.

3.2. i.MX 8M Plus SOM Connectors Mechanicals

On a baseboard, the i.MX 8M Plus SOM is installed into four 100-pin Hirose DF40 series 0.4mm-pitch board-to-board connectors. The exact part number of the connectors J3 – J6 are Hirose DF40C-100DP-0.4V(51).

The recommended mating connectors for a baseboard is the Hirose DF40HC(3.0)-100DS-0.4V(58) connectors, which provides 3mm stacking height for the i.MX 8M Plus SOM. The maximum height of the SOM above a baseboard for 3mm stacking height is 5.8mm.

3.3. i.MX 8M Plus SOM Top and Bottom Views

The following pictures provide the top and bottom views of the i.MX 8M Plus SOM:

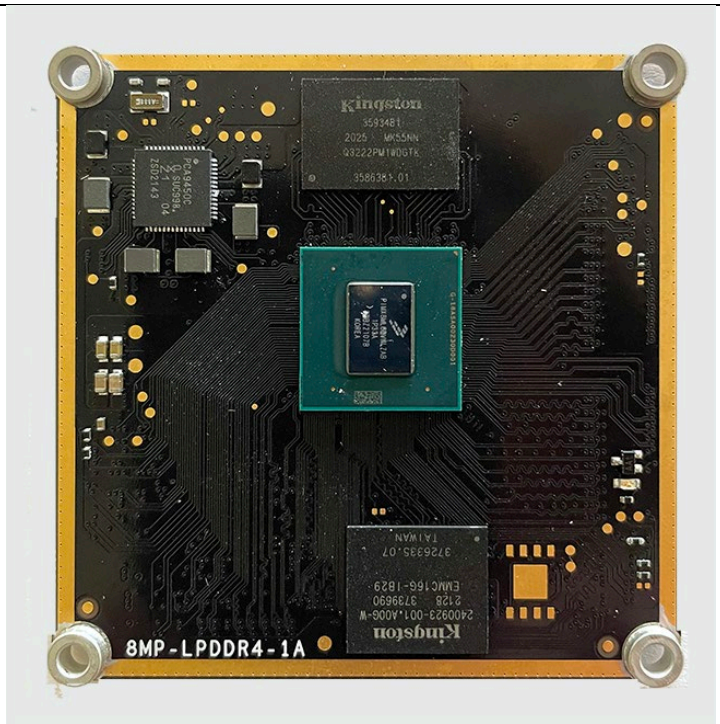

Figure 3: i.MX 8M Plus SOM Top View

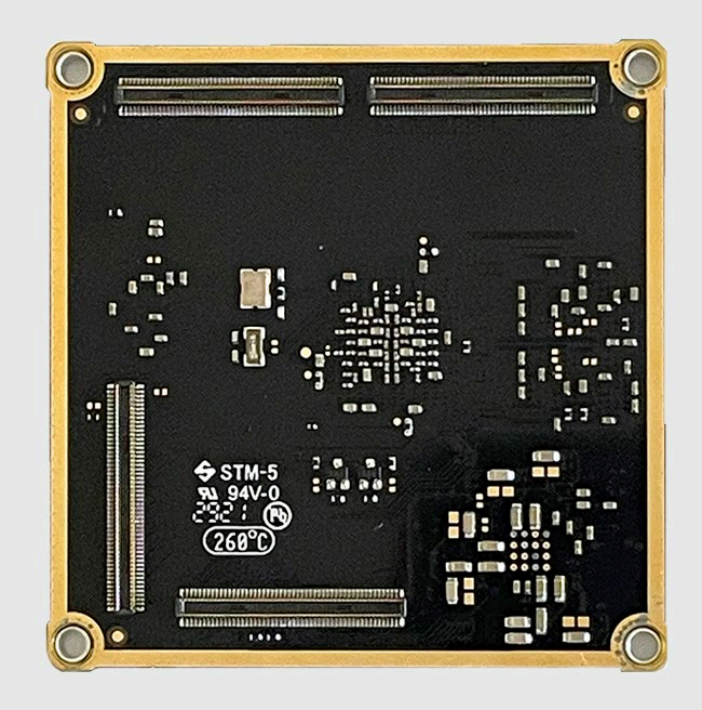

Figure 4: i.MX 8M Plus SOM Bottom View

4. Environment Specifications

4.1. Recommended Operating Conditions

The following table lists the recommended operating conditions of the i.MX 8M Plus SOM:

Symbol	Parameter	Range	
T_A	Ambient temperature	Commercial	0 to +70 ºC
VSYS_5V	+5V power supply	+5V +/-5%	

Table 1: Recommended Operating Conditions

5. Document Revision History

Revision	Date	Changes Summary
1.0	June 21, 2023	Initial version